TECHNICAL REQUIREMENTS

COMMON CAMERA DESIGN

CCD REQUIREMENTS

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1. Introduction

This note outlines the basic design requirements for the STEREO/SECCHI CCD imaging detectors.

These design requirements have been derived from the science and program requirements presented in the proposal entitled "Sun Earth Connection Coronal and Heliospheric Investigation" which was submitted to NASA on 27 July 1999 in response to AO 99-OSS-01 STEREO. The primary objective of this specification is to minimise the risk in the design of the SECCHI camera electronics, and ensure optimal operation within the SECCHI instruments.

The SECCHI science objectives are achieved with a mixture of instrumentation. Some aspects of the SECCHI science objectives require observations in the extreme ultraviolet (EUV) and some require observations in the visible wavelength ranges. For the purpose of this specification, the EUV regime consists of radiation in the wavelength range of 15-30 nm and the visible light regime consists of radiation in the wavelength range of 650-750 nm. Detectors optimised for each of these observational regimes will be required.

2. CCD Format and Pixel Size

2.1 Requirements:

1. The CCD format should be 2048 x 2048 configured in a full-frame readout mode.
2. The pixel pitch should be 13.5 microns to 12.0 microns.

2.2 Justifications:

1. Image format specified for the SECCHI instruments.
2. To match the plate-scale of the CCD detector to the optical design of the SECCHI instruments.

3. CCD Responsivity

3.1 Requirements:

1. The proposed CCD fabrication process must be capable of producing devices with a Detected Quantum Efficiency (DQE) of greater than 60% in the wavelength range of 15 – 30 nm for the EUV optimised CCDs; and greater than 80% in the wavelength range of 650 - 750 nm for the visible light optimised CCDs.
2. The choice of wavelength range (visible or EUV) for a given device must depend only upon the surface treatment of that device.
3. The proposed CCD fabrication process must be capable of producing devices such that the DQE of a typical EUV optimised CCD pixel will not change by more than 20% following an exposure to 10^{11} EUV photons.
4. Evidence that the CCD response requirements can be met must be provided in the proposal. This may be demonstrated through testing by the vendor, or by the vendor's customers, providing that the information provided is sufficient to evaluate the testing techniques and results.

3.2 Justifications:

1. The scientific requirements of image exposure time and the mission restriction on aperture constrain the minimum DQE.
2. Minimisation of delivery risk, and the demands on testing to optimise the performance of an individual camera place the requirement on device commonality between the EUV and visible devices.
3. Projections of the SECCHI EUVI instrument operations indicate a EUV photon flux exceeding 10^{11} photons per pixel, and the scientific requirements constrain the DQE stability.
4. Minimisation of programme risk in an accelerated project delivery programme requires that all the response performance be demonstrated by previous work by the vendor or by customers at the time of proposal.

4. CCD Clock Voltages and Clock Phases

4.1 Requirements:

1. All CCD drive clocks must be referenced to a lower clock voltage level of 0 V in order to ease the design, and minimise the size of the camera's low power clock driver circuitry. It should not be a necessity to set the lower voltage level of the CCD's imaging area (or parallel register) clock phases either more positive, or more negative than the lower voltage level of the serial output register clock phases in order to achieve optimal operation and charge transfer efficiency.
2. All CCD drive clocks should achieve optimal full well capacity and charge transfer efficiency with clock swings of ≤ 14 V.
3. Both the parallel and serial registers must operate with 3-phase clocking sequences (excluding summing gates).
4. The serial output register design must incorporate nominally identical output amplifiers at each end of the register. It must be possible to read the CCD out through either amplifier, or both amplifiers simultaneously (i.e. split-register operation) simply by altering the timing of the serial register clock-phase sequencing.

Summary

Description	Lower level (V)	Upper level (V)	Comments
Imaging area (parallel register) drive clocks	0	≤ 14	For optimal operation.
Output register (serial register) drive clocks	0	≤ 14	For optimal operation.
Output amplifier reset clock	0	≤ 14	For optimal operation.
Summing wells	0	≤ 14	For optimal operation.

4.2 Justifications:

1. To ease the design, and minimise the size of the camera's low power clock driver circuitry. Both the parallel imaging area and serial output registers will be driven from a digital sequencer with simple level-translator circuitry (e.g. MOSFET driver ICs) to achieve the necessary drive clock amplitude. The SECCHI cameras will exploit design and qualification heritage from the RAL Solar Mass Ejection Imager (SMEI) cameras.
2. To ease the design, and minimise the size of the camera's low power clock driver circuitry. The upper voltage level of the CCD's drive clocks will be derived from a 15 V supply. Allowing for some voltage drop across the regulation circuitry, this dictates that the maximum drive clock amplitude must be ≤ 14 V. The SECCHI cameras will exploit design and qualification heritage from the SMEI cameras.
3. To minimise the number of drive clock channels required.
4. Dual-port CCD readout is required; firstly to allow increased frame readout rate in some SECCHI operating modes, and secondly to provide some measure of redundancy. Single or dual-port readout operation must be programmable from the ground.

5. Full Well Capacity

5.1 Requirements:

1. The CCD full well capacity in the imaging area (parallel register) pixels must be ≥ 100k electrons.
2. The CCD serial output register and output amplifier operation must have a dynamic range of four times the full well capacity.

5.2 Justifications:

1. SECCHI dynamic range requirement.
2. On-chip pixel binning of 2 x 2 pixels is required for some SECCHI readout modes. The serial output register and output amplifier operation must therefore have sufficient dynamic range to handle signals of four times the nominal pixel full well capacity.

6. CCD Charge Transfer

6.1 Requirements:

1. The imaging area parallel register charge transfer efficiency (CTE) must be ≥ 99.999% for clock periods of ≤ 50 μs per line transfer, and for low signal levels (<2% of full well as specified in section 5).
2. The serial readout register charge transfer efficiency (CTE) must be ≥ 99.999% for clock periods of ≤ 1 μs per pixel transfer, and for low signal levels (<2% of full well as specified in section 5).
3. All transfers must not reduce the specified minimum full well capacity, and hence signal dynamic range (see section 5).

6.2 Justifications:

1. The photometric precision requirements of all the instruments set the minimum CTE. The cadence requirements of the two SECCHI coronagraphs to obtain polarization brightness sequences sets the minimum clock rates for the CCD.
2. (see 1. above).
3. To maintain the minimum specified signal dynamic range.

7. CCD Bias Voltages

7.1 Requirement:

1. All CCD bias voltages must lie in the range 0 V ≤ bias voltage ≤ 31 V.

7.2 Justification:

1. To ease the design, and minimise the size of the camera's low power drive circuitry. The SECCHI cameras will exploit design and qualification heritage from the RAL SMEI cameras.

8. CCD Output Amplifier

8.1 Requirements:

1. The CCD output amplifier must be capable of achieving ≤ 8 electrons rms with clamp-sample correlated double sampling at a pixel readout rate of 1 Mpixel/s.
2. The CCD output amplifier must provide an output sensitivity ≥ 3 μV/electron.
3. Overall, the CCD output amplifier must be capable of driving 20 cm of cable directly before pre-amplification, while maintaining a readout noise of ≤ 8 electrons rms at a readout rate of 1 Mpixel/s. The CCD output amplifier output impedance must be ≤ 500 ohms during readout at the rate of 1Mpixel/s and at a device temperature of –50°C.

8.2 Justifications:

1. The CCD readout noise specification, and the pixel readout rate requirement result from the overall SECCHI scientific requirements of image exposure time and the mission restriction on aperture.
2. The SECCHI CCDs will all be controlled from dedicated camera electronics units. Three CCDs within the SECCHI Solar Coronal Imaging Package (SCIP) instruments will be driven from one controller. Two CCDs within the two cameras of the SECCHI Heliospheric Imager (HI) instrument will be driven from a second controller. There will be no pre-amplification in the focal planes, and therefore there is a requirement for the CCD output amplifier to have good drive capability.
3. (see 2. Above) The minimum cable length is dictated by the locations of the camera focal planes within the SCIP and HI instruments. The device impedance requirement is derived from this cable length drive requirement and the analog electronics design approach.

9. Dark Current

9.1 Requirements:

1. The dark current must be ≤ 2 nA/cm^2/s (24,000 electrons per pixel/s) at 20°C.

9.2 Justifications:

1. Standard non-inverted mode CCDs are anticipated to have greater full well capacity, and thus a greater signal dynamic range. However, laboratory testing in air is sometimes necessary and the dark current must be low enough to achieve some imaging with sufficiently specialised ROI and readout clocking.

10. CCD Dump Drain

10.1 Requirements:

1. The CCD output register must incorporate an adjacent dump drain to allow for rapid clearing of the chip. If an alternative CCD clearing approach is proposed, it should be comparable to the dump drain architecture in speed and efficiency.

10.2 Justifications:

1. Some SECCHI instrument operating modes require rapid clearing of the CCD prior to the next exposure. A gated dump drain is required in order to maximise how fast charge can be cleared and dumped from the CCD imaging area (parallel registers). Hence, in order to clear the chip prior to an exposure, it should not be necessary to read out the serial output register in order to remove the unwanted charge.

11. Flatness

11.1 Requirements:

1. The CCD chip should be flat across its imaging surface to ≤ 40 μm at an operating temperature of -50°C. The CCD package to be integrated into the instrument focal plane must have a system of references (marks, surfaces, pins, etc.) which allow the mean CCD imaging surface to be aligned with the instrument focal plane to ≤ 20 μm at an operating temperature of -50°C.

11.2 Justifications:

1. SECCHI optical design requirement.

12. Double-sided Anti-static Gate Protection

12.1 Requirements:

1. The CCD should incorporate double-sided anti-static gate protection in order to minimise the chance of accidental damage.

12.2 Justifications:

1. Minimisation of risk of damage to SECCHI CCD chips during test, integration, or adverse operation.

13. CCD Defects

13.1 Requirements:

1. Less than 300 hot pixels (of >10x the dark current specified in section 9), or dark pixels (of <50% of the median response). Specifications are for –50 °C CCD operating temperature.
2. Less than 20 traps deeper than 250 electrons. Specifications are for –50 °C CCD operating temperature.
3. Less than or equal to 4 column blemishes (of >64 contiguous defective pixels). Specifications are for –50 °C CCD operating temperature.

13.2 Justifications:

1. The efficiency of the image compression algorithms under consideration for SECCHI is severely compromised by CCD defects. The onboard computational resources are limited by the mass and power constraints of the STEREO mission.
2. See Note 1. above.
3. See Note 1. above.

14. Packaging

14.1 Requirements:

1. The CCD packaging should be consistent with the SECCHI focal plane packaging concept developed for the SECCHI Phase A Feasibility Study Report. A preliminary version of that concept, sufficient for the purposes of this specification, is included below (Figure 1). Additional features, of demonstrated value in a cost-constrained spacefilght program, may be proposed to achieve one or more of the following: improve thermal efficiency, reduce mass, reduce volume, improve the ease of integration and test, reduce delivery risk, and reduce overall program cost. Each additional feature should be listed individually, with benefits and costs specific to each.

14.2 Justification:

1. Minimum redesign of a concept that has already gone through an optimisation of thermal properties. Since it is possible that repackaging a device into an application specific unit can improve the overall program efficiency, such a proposal will be considered - providing that the repackaging is based on previously proven approaches and is not an open-ended development program.

15. Quality Assurance

1. A minimum quality assurance program comparable to ISO-9000 is required. Each CCD must be marked with lot number and device number to allow traceability to the device's batch, wafer, and position on the wafer. Additional quality assurance tasks, of demonstrated value in cost-constrained spaceflight programs, may be offered either to reduce the CCD evaluation and acceptance testing at NRL, to reduce programmatic risk, or to otherwise reduce overall program cost. These tasks should be listed individually, with benefits and cost specific to each. Documentation of the QA program is a required deliverable of the CCD program.

15.1 Optional Quality Assurance Program:

1. In addition to the above quality assurance proposal, the contractor shall provide the cost of one specific enhancement to the baseline quality assurance, an extended burn-in test for the flight devices. The temperature of the burn-in should be +125 and the duration should be 80 hours. No tracking of electrical parameter drifts is necessary during the burn-in. The biases should be set to the maximum level. This extended burn-in should be conducted in place of the commercial baseline burn-in. The optical and electrical testing and the test documentation should be the same as the commercial baseline program.

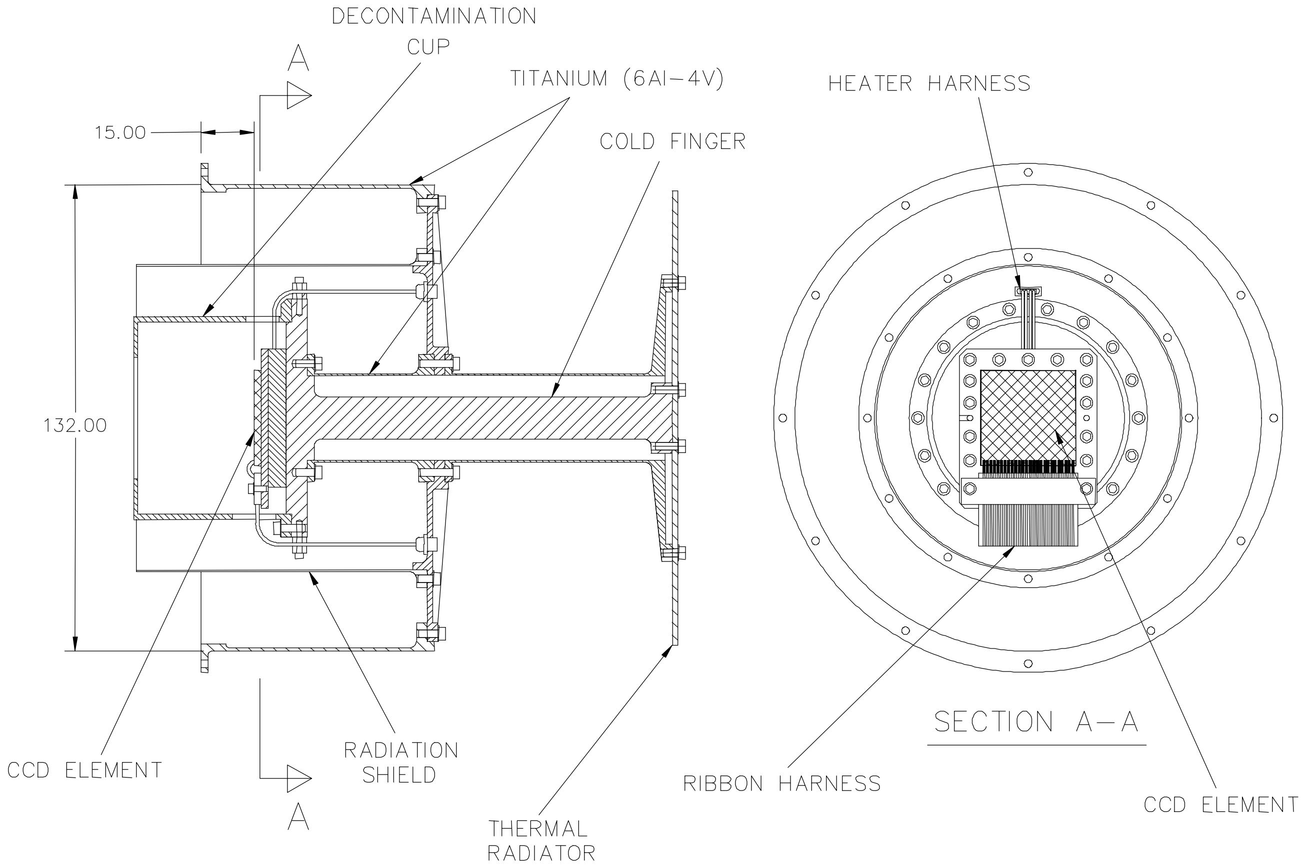

Figure 1. SECCHI Focal Plane Packaging Concept

SECCHI focal plane packaging concept developed for the SECCHI Phase A Feasibility Study Report.