

## **SIMOX Wafer Specification**

### **1.0 Scope**

This specification defines substrate material and criteria to be met or exceeded by the suppliers of annealed SIMOX (Separation by Implantation of Oxygen) SOI (Silicon on Insulator) wafers.

### **2.0 Applicable Documents**

The following documents form a part of this specification:

#### **2.1 ANSI Standards (most recent revision)**

ASME B46.1 Surface Texture (Surface Roughness, Waviness, and Lay)

#### **2.2 ASTM Standards (most recent revision)**

F1188 Test Method for Interstitial Atomic Oxygen Content of Silicon by Infrared Absorption

F1391 Test Method for Substitutional Atomic Carbon Content of Silicon by Infrared Absorption

#### **2.3 Military Standards (most recent revision)**

MIL-STD-105 Sampling Procedures and Tables for Inspection by Attributes

MIL-STD-414 Sampling Procedures and Tables for Inspection by Variables for Percent Defective

#### **2.4 SEMI Standards (most recent revision)**

SEMI International Standards - Materials

SEMI M1 Specifications for Polished Monocrystalline Silicon Wafers

SEMI M1.8 Standard for 150 mm Polished Monocrystalline Silicon

### **3.0 SIMOX Wafer Requirements**

The following criteria must be met by the supplier. Inspection methods are given for reference purposes. Inspection methods that contact or alter any film or defect shall not be performed on supplied wafers.

The complete specification for this product includes all general requirements of SEMI M1 Specifications for Polished Monocrystalline Silicon Wafers and SEMI M1.8 Standard for 150 mm Polished Monocrystalline Silicon Wafers, including thickness, TTV, bow and warp, except where specified in this document.

Specifications of Specific Wafer Requirements supersede specifications of General Properties. The specific requirements for 200 mm Diameter Advantox® MLD Wafers are described in Section 4. The specific requirements for 150 mm Diameter Advantox® MLD Wafers are described in Section 5. The specific requirements for 150 mm Diameter Advantox® 150 Wafers are described in Section 6. The additional silicon implant for reliability improvement to be applied to all of the completed wafers is described in Section 7.

#### 4.0 Specific Properties of 200 mm Diameter Advantox® MLD Wafers

Electrical Characteristics, Substrate	Units	Max		Min	Ref
Conductivity Type	Pos/Neg		Pos		
Resistivity Average	$\Omega$ -cm	18		9	
Resistivity Deviation	%	14			

Orientalional Characteristics, Substrate	Units	Max		Min	Ref
Surface Projection	Miller Indicies		(100)		
Surface Declination	Deg. Collat.	1		0	
Notch Azimuth	Deg. Long.	95		85	

Electrical Si, and Oxide	Units	Max		Min	Ref
Electron Mobility, Superficial Layer	$\text{cm}^2/\text{V-sec}$			700	
Hole Mobility, Superficial Layer (reference only)	$\text{cm}^2/\text{V-sec}$			150	
Transconductance (GME) @ 12V	$\mu\text{A}/\text{V}$			800	
Output Conductance @ 2HRS	$\mu\text{A}/\text{V}$	100			
Drain Linear Conductance (reference only)	$\mu\text{A}/\text{V}$			350	
Oxide Charge (QBOX)	$\text{cm}^{-2}$	3.5E11			
Interface State Density (DIT) (reference only)	$\text{cm}^{-2}/\text{eV}$	3.5E11			
Dopant Concentration, Superficial Layer ( $N_A$ )	$\text{cm}^{-3}$	2E16			
Buried Oxide Shorts	$\text{cm}^{-2}$	1			
Average 1 <sup>st</sup> Mini Breakdown Voltage (V1bd)	V			50	
1 <sup>st</sup> Mini Breakdown Yield @ 50V	%			90	
Median Leakage Current @ 2MV/cm (0.05 $\text{cm}^2$ dot)	nA	0.5			

<b>Topographical Characteristics</b>	<b>Units</b>	<b>Max</b>		<b>Min</b>	<b>Ref</b>
Area Defects $\geq 1.6\mu\text{m}$ (OOB)	#	10			
Light Point Defects $\geq 0.3\mu\text{m}$ (OOB)	#	350			
Light Point Defects $\geq 0.16\mu\text{m}$ (OOB)	#	TBD			
Edge Chips, Peripheral $> 0.15\text{ mm}$	#	0			
Edge Chips, Surface $> 0.15\text{ mm}$ (Front)	#	0			
Edge Chips, Surface $> 0.15\text{ mm}$ (Rear)	#	0			
Scratches, Front/Rear	#	0			
Cracks, Front/Rear	#	0			
Haze, Front	%	0			
Contaminants, Front/Rear	Area%	0			
Blemishes, Front	Area%	0			
Roughness, Rear	$\mu\text{m}$	0.5			
Roughness, Edge	$\mu\text{m}$	0.06			
Sawmarks, Front	#	0			
Orange Peel, Front	Area%	0			

<b>Dimensional Characteristics, Substrate</b>	<b>Units</b>	<b>Max</b>		<b>Min</b>	<b>Ref</b>
Thickness	$\mu\text{m}$	745		705	
Parallelism	$\mu\text{m}$	10			
Warpage	$\mu\text{m}$	60			
Flatness, SFQR Max	$\mu\text{m}$	0.5			
Site Flatness $\leq 0.3\ \mu\text{m}$ (SFQR 25x25mm PSA)	Area%			85	
Global (TIR)	$\mu\text{m}$	5			
Notch Depth	mm	1.25		1	
Notch Form					IBM Spec 2412428
Wafer Radius	mm	100.125		99.875	
Edge Contour					IBM Spec 2412428
Bow	$\mu\text{m}$	60			

<b>Dimensional Characteristics, Si Layer, BOX</b>	<b>Units</b>	<b>Max</b>		<b>Min</b>	<b>Ref</b>
Superficial Silicon Layer Thickness, Mean +/- 3 Sigma	$\mu\text{m}$	0.1545		0.1355	
Box Thickness Average	$\mu\text{m}$	0.151		0.124	

<b>Crystal Properties, Superficial Si Layer</b>	<b>Units</b>	<b>Max</b>		<b>Min</b>	<b>Ref</b>
Dislocation Edge Pit Density	cm <sup>-2</sup>	5E6			
HF Defect Density	cm <sup>-2</sup>	7			
Slip (5mm Edge Exclusion) (Reference Only)	#	10			
Surface Roughness, 10µm x 10µm	Å	10			AFM
Surface Mounds Density, 10µm x 10µm	cm <sup>-2</sup>	1E6			AFM
Surface Pit Density, 10µm x 10µm	cm <sup>-2</sup>	1E6			AFM
Edge Damage	Area%	0			

<b>Serialization Characteristics</b>	<b>Units</b>	<b>Max</b>		<b>Min</b>	<b>Ref</b>
Product Code	Identity		Y		
Location					IBM Spec 57X9049
Machine Readable Backside Barcode	%Read			100	
Man Readable Backside OCR	%Read			100	

<b>Compositional Characteristics</b>	<b>Units</b>	<b>Max</b>		<b>Min</b>	<b>Ref</b>
Doping Element	Identity		Boron		
Oxygen, Interstitial Concentration (Substrate)	ppma	28		20	
Surface Metals (Fe, Cu, Ni, Zn, Cr, Na, Ca)	cm <sup>-2</sup>	1E11			
Surface Metals (K, Al)	cm <sup>-2</sup>	5E11			
Silicon On Insulator Metals (Reference Only) (Cu)	cm <sup>-2</sup>	5E11			
Silicon On Insulator Metals (Reference Only) (Fe, Ni, Zn, Cr, Na, Ca, Al)	cm <sup>-2</sup>	1E11			

### 5.0 Specific Properties of 150 mm Diameter Advantox® MLD Wafers

All Requirements of SEMI M1 Specification for Polished Monocrystalline Silicon Wafers and SEMI M1.8 Standard for 150 mm Polished Monocrystalline Silicon Wafers, including thickness, TTV, bow and Warp, shall be met, except where specified as follows:

Parameter	Limit	Method
5.1 Nominal Edge Exclusion	6 mm	
5.2 Wafer Site Flatness		
Site Map		Standard Map
Site Flatness SFQD	$\leq 0.25 \mu\text{m}$	
Site Size	22 mm by 22 mm	
SFQD Edge Exclusion	3 mm	
5.3 Total Indicator Reading	$\leq 3.0 \mu\text{m}$	80% of wafer area
5.4 Adhering Particulate Matter	$\leq 0.20/\text{cm}^2$	$\geq 0.4 \mu\text{m}$ Tencor 6400 or equivalent
5.5 Front Surface Oxide	None	
5.6 Back Surface Oxide	None	
5.7 Back Surface Roughness	$\leq 1.27 \mu\text{m RMS}$	ANSI/ASME B46.1
5.8 Device Silicon Layer Properties		
5.8.1 Surface Micro Roughness	$\leq 10.0 \text{ \AA RMS}$	AFM scan size: $5 \times 5 \mu\text{m}$
5.8.2 Oxygen Content	<detection limit	ASTM F 1188
5.8.3 Metallic Contamination, per each element: Ti, Cr, Fe, Co, Ni, Cu, Zn Fe, Ni, Cu, Al, Mo	$\leq 5 \times 10^{10}/\text{cm}^2$ $\leq 1 \times 10^{11}/\text{cm}^2$	TXRF AAS
5.8.4 Carbon Contamination	$\leq 0.5 \text{ ppma}$	ASTM F 1391
5.8.5 N-type Dopant Concentration and P-type Dopant Concentration (at Device Silicon Layer midpoint)	$\leq 5 \times 10^{15}/\text{cm}^3$	SIMS
5.8.6 Dislocation Defect Density	$\leq 1 \times 10^9/\text{cm}^2$	Modified SECCO etch
5.8.7 HF Defects	$\leq 2.0/\text{cm}^2$	Each wafer $\geq 10 \text{ min}$ , 49% HF etch
	$\leq 1.0/\text{cm}^2$	Each wafer $\geq 0.4 \mu\text{m}$ KLA 2122 or equivalent
	$> 0.5/\text{cm}^2$	$\leq$ one wafer per batch, $\geq 0.4 \mu\text{m}$ KLA 2122 or equivalent
5.8.8 Other Defect Density	$\leq 1.5/\text{cm}^2$	$\geq 0.4 \mu\text{m}$ KLA 2122 or equivalent

**5.8.9 Gate Oxide Integrity**

A comparison between coprocessed SOI SIMOX and non-SOI wafers, where the non-SOI wafers meet all other applicable requirements in section 3.0, shall show no statistically significant difference between the breakdown voltage histograms of capacitors with 150 Å pyrogenic SiO<sub>2</sub> grown on the top Si layer. (Note, the capacitors should be measured in accumulation.) The ramp-voltage breakdown test with a ramp rate of 2MV/sec shall be used to determine the gate oxide breakdown voltage. The breakdown voltage is defined to be that voltage, V<sub>BD</sub>, at which either the conductance of the 150 Å SiO<sub>2</sub> suddenly increases (i.e. the current density through the gate oxide capacitor is larger than 1 A/cm<sup>2</sup>.)

5.8.10	Thickness (mean)	1450 Å ±50 Å	
5.8.11	Thickness Uniformity	<= 100 Å	
5.9	Buried Oxide Layer Properties		
5.9.1	Thickness (mean)	1300 Å ±100 Å	
5.9.2	Thickness Uniformity	<= 150 Å	
5.9.3	Pin Hole Density	<= 0.10/cm <sup>2</sup>	CuSO <sub>4</sub> Plating
		<= 0.5/cm <sup>2</sup>	> 100 nA @ 50V Probed Cap

### 6.0 Specific Properties of 150 mm Diameter Advantox® 150 Wafers

All Requirements of SEMI M1 Specification for Polished Monocrystalline Silicon Wafers and SEMI M1.8 Standard for 150 mm Polished Monocrystalline Silicon Wafers, including thickness, TTV, bow and Warp, shall be met, except where specified as follows:

Parameter	Limit	Method
6.1 Nominal Edge Exclusion	6 mm	
6.2 Wafer Site Flatness		
Site Map		Standard Map
Site Flatness SFQD	$\leq 0.25 \mu\text{m}$	
Site Size	22 mm by 22 mm	
SFQD Edge Exclusion	3 mm	
6.3 Total Indicator Reading	$\leq 3.0 \mu\text{m}$	80% of wafer area
6.4 Adhering Particulate Matter	$\leq 0.20/\text{cm}^2$	$\geq 0.4 \mu\text{m}$ Tencor 6400 or equivalent
6.5 Front Surface Oxide	None	
6.6 Back Surface Oxide	None	
6.7 Back Surface Roughness	$\leq 1.27 \mu\text{m RMS}$	ANSI/ASME B46.1
6.8 Device Silicon Layer Properties		
6.8.1 Surface Micro Roughness	$\leq 10.0 \text{ \AA RMS}$	AFM scan size: $5 \times 5 \mu\text{m}$
6.8.2 Oxygen Content	<detection limit	ASTM F 1188
6.8.3 Metallic Contamination, per each element: Ti, Cr, Fe, Co, Ni, Cu, Zn Fe, Ni, Cu, Al, Mo	$\leq 5 \times 10^{10}/\text{cm}^2$ $\leq 1 \times 10^{11}/\text{cm}^2$	TXRF AAS
6.8.4 Carbon Contamination	$\leq 0.5 \text{ ppma}$	ASTM F 1391
6.8.5 N-type Dopant Concentration and P-type Dopant Concentration (at Device Silicon Layer midpoint)	$\leq 5 \times 10^{15}/\text{cm}^3$	SIMS
6.8.6 Dislocation Defect Density	$\leq 1 \times 10^6/\text{cm}^2$	Modified SECCO etch
6.8.7 HF Defects	$\leq 2.0/\text{cm}^2$	Each wafer $\geq 10 \text{ min}$ , 49% HF etch
	$\leq 1.0/\text{cm}^2$	Each wafer $\geq 0.4 \mu\text{m}$ KLA 2122 or equivalent
	$> 0.5/\text{cm}^2$	$\leq$ one wafer per batch, $\geq 0.4 \mu\text{m}$ KLA 2122 or equivalent
6.8.8 Other Defect Density	$\leq 1.5/\text{cm}^2$	$\geq 0.4 \mu\text{m}$ KLA 2122 or equivalent

**6.8.9 Gate Oxide Integrity**

A comparison between coprocessed SOI SIMOX and non-SOI wafers, where the non-SOI wafers meet all other applicable requirements in section 3.0, shall show no statistically significant difference between the breakdown voltage histograms of capacitors with 150 Å pyrogenic SiO<sub>2</sub> grown on the top Si layer. (Note, the capacitors should be measured in accumulation.) The ramp-voltage breakdown test with a ramp rate of 2MV/sec shall be used to determine the gate oxide breakdown voltage. The breakdown voltage is defined to be that voltage, V<sub>BD</sub>, at which either the conductance of the 150 Å SiO<sub>2</sub> suddenly increases (i.e. the current density through the gate oxide capacitor is larger than 1 A/cm<sup>2</sup>.)

6.8.10	Thickness (mean)	1900 Å ±50 Å	
6.8.11	Thickness Uniformity	≤ 100 Å	
6.9	Buried Oxide Layer Properties		
6.9.1	Thickness (mean)	1500 Å ±100 Å	
6.9.2	Thickness Uniformity	≤ 150 Å	
6.9.3	Pin Hole Density	≤ 0.10/cm <sup>2</sup>	CuSO <sub>4</sub> Plating
		≤ 0.5/cm <sup>2</sup>	> 100 nA @ 50V Probed Cap

## **7.0 Additional Silicon Implant for Reliability Improvement**

After the completion of the SIMOX wafer fabrication process, each wafer shall receive an additional high dose silicon implant and anneal for reliability improvement purposes. The details of the silicon implant and anneal will be provided by the Naval Research Laboratory on request.

## **8.0 Quality Assurance Provisions**

### **8.1 Acceptance of Material**

All material lots shall be accompanied by a certificate of conformance which guarantees the material parameters listed in Section 3.0 and lists the manufacturer's lot designation. If the certificate of conformance is not received within 24 hours of delivery, the material will not be accepted. In addition, the manufacturer shall supply actual test results on the following parameters which are listed in Section 3.0:

- Device Silicon Layer Thickness
- Device Silicon Layer Thickness Uniformity
- Device Silicon Layer HF Defect Density
- Buried Oxide Layer Thickness or Oxygen Implant Dose
- Buried Oxide Layer Thickness Uniformity or Oxygen Implant Dose Uniformity
- Buried Oxide Layer Pinhole Density
- Other Defect Density
- Metallic Contamination

### **8.2 SIMOX Process Data**

The supplier shall supply contamination and defect data including (1) Buried Oxide Layer defect data, (2) TXRF data of SIMOX wafer background contamination, and (3) particle counts on front surface of annealed SIMOX wafer.

### **8.3 Procedures**

The manufacturer shall draw samples and conduct analysis, using the most current ANSI, ASTM, Military, or SEMI standard methods, or equivalents, to guarantee the requirements listed in Section 3.0. The manufacturer may use in-line statistical process control data to guarantee conformance of the material.

## **9.0 Preparation for Delivery**

### **9.1 Containers**

Containers shall be selected to protect material and personnel during normal shipping and handling operations. Material shall be packed in containers which protect the material from outside contamination and which minimize abrasive contact with the polished side of the wafer.

Containers may be any one of a number normally used by the silicon wafer manufacturing industry.

## 9.2 Marking

The container labeling shall include the manufacturer's identification, material name, the quantity, manufacturer's lot designation, and any precautionary information as a minimum. This information shall be durably and legibly marked on each container.

## 9.3 Shipping and Storage

The material shall be shipped and stored under conditions which allow the material to maintain the properties listed in section 3.0.

## 10.0 Notes

10.1 Metric, although not herein binding, is to be considered the preferred system of measurement.

10.2 Particulate matter will be considered adhering if it remains after a spin dry or comparable rinse.