

Specification for Reconfigurable Signal Processor Development System

This order is for the purchase of items constituting a Reconfigurable Signal Processor Development System. The system hardware will incorporate hardware signal processors using field programmable gate arrays (FPGAs).

The hardware required for the development system must include the following items:

1. Wideband Analog-to-Digital Converter (ADC) card (Quantity 1)

The card specification is as follows:

- a. Incorporates one MAX108 1.5 GSPS (gigasample per second), 8-bit ADC.
- b. 4 Mbyte FIFO for data capture.
- c. Two Xilinx Virtex-II Pro XC2VP50 FPGAs for signal processing.
- d. Each FPGA has two banks of 128 Mbyte DDR SDRAM.
- e. Dual RACE++ backplane interface.
- f. External clock, sync and trigger inputs to allow synchronization of multiple boards.
- g. Front-panel 16-bit RapidIO connector for streaming ADC data off the card.
- h. Triggering mode that makes board trigger on the next sync clock edge after a trigger is detected.
- i. 6U VME-64X card spec with a VXS P0 connector containing 8 bidirectional high-speed serial links.

2. Narrowband ADC card with wideband digital receivers.

The specification for this card is as follows:

- a. Incorporates four 14-bit, 105 MSPS ADCs.
- b. Each ADC is followed by a digital down converter (DDC) that supports high fidelity sample rate reductions by factors of 2 to 8.
- c. Two Xilinx Virtex-II Pro XC2VP50 FPGAs for signal processing.
- d. Each DDC is followed by a 256 Kbyte Quad Port SRAM buffer to pass data to the Xilinx FPGAs.
- e. Each FPGA has two banks of 256 Mbyte DDR SDRAM.
- f. Dual RACE++ backplane interface.
- g. External clock, sync input and sync output signals provided on SMA connectors
- h. Front-panel 16-bit RapidIO connector for streaming ADC data off the card.
- i. 6U VME-64X card spec with VXS P0 connector containing 8 bidirectional high-speed serial links.

3. FPGA Prototyping card (Quantity 1)

The card specification is as follows:

- a. PCI/PCI-X card form factor.
- b. Single Xilinx Virtex-II Pro XC2VP70-7 FPGA.
- c. Four external banks of 4 Mbyte pipeline ZBT Static RAM.
- d. Four external banks of 32 Mbyte DDR SDRAM.
- e. 10 high-speed serial ports utilizing the internal MGTs of the FPGA. The ports are configured as four channels of fiber Gigabit Ethernet, 2 SATA connectors, 2 HSSDC2 connectors and 2 channels with SMA connectors.
- f. One 200-pin high-speed connector.